EE/CprE/Se 492 Weekly Report 1
End of EE/CprE/Se 491- 1/31/25
sdmay25-28
Digital ASIC fabrication
Client & Advisor: Dr. Duwe

Team Members
Calvin Smith – Accelerator Design lead
Camden Fergen – DevOps and Project Lead
John – Testing Lead
Nicholas – Harden and Verification lead
Levi – Communication Interfaces Lead

Weekly Summary

This week we were able to work on some components that will be making up our CyGRA accelerator. While designing those components we were also able to create some testbenches for those designed components.

Pask Week Accomplishments

- Calvin:
  - Implemented the processing element for the CyGRA in verilog along with subcomponents
- Camden:
  - Planned out the team meetings and the schedule for the semester
  - Started to put together schedule for this semester to ensure team stays on track
  - Managed tasks and assigned to various team members to ensure work was being completed
- John:
  - Worked on writing test benches for some parts of the accelerator
    - Made testbench for adder, multiplier, and processing element
  - Created my own small efabless project to be able to properly learn the tools and contribute more
- Levi:
  - Finding benchmarks and running benchmarks on the pico processor
- Nicholas:
  - Create Wishbone Slave unit

- Integrated Wishbone Slave, Pico, Memory Controller, Memory, and Cache into one top level verilog module for testing.
- Ran tests on the created top level design.

Name	Individual Contribution	Hours this Week	Hours Cumulative
Calvin	• Verilog fun times • Processing element implementation	5	82.044
Camden	• Gantt chart update • Planning for semester • Team management	4	68
John	• Multiple testbenches • Small efabless project	8	72
Levi	• Pico benchmarks	4	68
Nicholas	• Wishbone Slave • Top Level Design • Top Level Tests	10	90

Plans for Upcoming Week

- Calvin:
  - Begin and perhaps finish the top-level design entity instantiating the processing elements
  - Define interfaces for subcomponents needed for governing PEs
  - Create instruction definitions and begin parser
- Camden:
  - Guide team to create block diagram consisting of all the separate modules and interconnects planned
    - Ensure the team members can connect modules together during integration

    - Finish gantt chart planning and converse with team to ensure its correct and accurate based on timing
    - Prepare for next Advisor meeting as well as instructor meeting
- John:
    - Continue with writing testbenches and working with the efabless tools
- Levi:
    - Help write testbenches and find standardized benchmarks
- Nicholas:
    - Finish Testing Memory Controller.
    - Finalize Memory and Cache selection.
    - Begin Hardening complete modules.

<u>Summary of weekly advisor meeting</u>

Met with Dr Duwe and went over any progress we had made since our last meeting (end of 491). Showed off progress made on memory/cache system as well as provided an update on current status of aspects of the project. Additionally, Duwe laid out some of the requirements for the rest of the semester as well as what is expected (bare min) at the end of the semester/April 11th efabless submission deadline